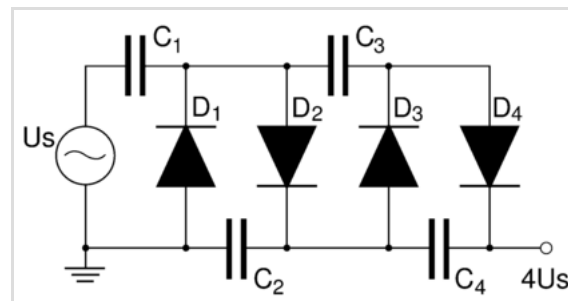# Voltage multiplier

A **voltage multiplier** is an electrical circuit that converts AC electrical power from a lower voltage to a higher DC voltage, typically using a network of capacitors and diodes.

Voltage multipliers can be used to generate a few volts for electronic appliances, to millions of volts for purposes such as high-energy physics experiments and lightning safety testing. The most common type of voltage multiplier is the half-wave series multiplier, also called the Villard cascade (but actually invented by Heinrich Greinacher).

Villard cascade voltage multiplier.

Operation

Assuming that the peak voltage of the AC source is $+U_s$, and that the C values are sufficiently high to allow, when charged, that a current flows with no significant change in voltage, then the (simplified) working of the cascade is as follows:

1. going from positive peak ($+U_s$) to negative peak ($-U_s$): The C_1 capacitor is charged through diode D_1 to U_s V (potential difference between left and right plate of the capacitor is U_s).
2. going from negative peak to positive peak: The voltage of C_1 adds with that of the source, thus charging C_2 to $2U_s$ through D_2 and discharging C_1 in the process.

Illustration of the described operation, with $+U_s$ = 100 V

3. positive to negative peak: Voltage of C_1 has dropped to 0 V by the end of the previous step, thus allowing C_3 to be charged through D_3 to $2U_s$.
4. negative to positive peak: Voltage of C_2 rises to $2U_s$ (analogously to step 2), also charging C_4 to $2U_s$. The output voltage (the sum of voltages of C_2 and C_4) rises until $4U_s$ is reached.
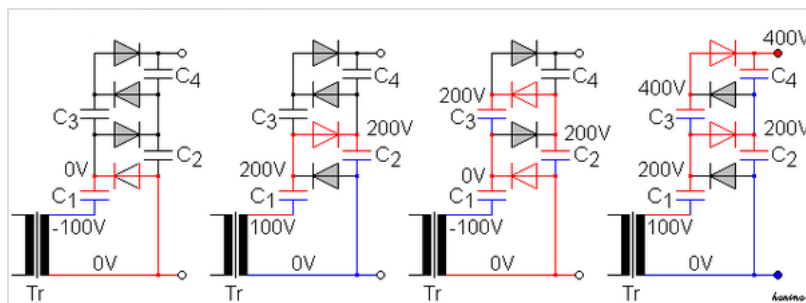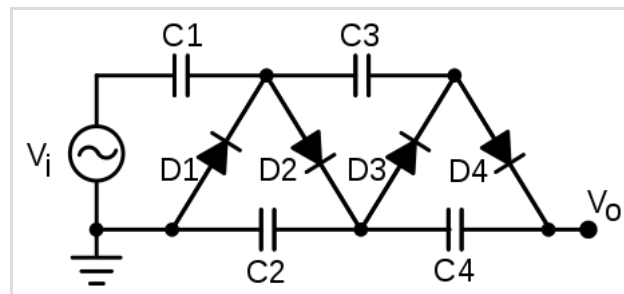
Adding an additional stage will increase the output voltage by twice the peak AC source voltage (minus losses due to the diodes – see the next paragraph).

In reality, more cycles are required for C_4 to reach the full voltage, and the voltage of each capacitor is lowered by the forward voltage drop (U_f) of each diode on the path to that capacitor. For example, the voltage of C_4 in the example would be at most $2U_s$ - $4U_f$ since there are 4 diodes between its positive terminal and the source. The total output voltage would be $U(C_2) + U(C_4) = (2U_s$ - $2U_f) + (2U_s$ - $4U_f) = 4U_s$ - $6U_f$. In a cascade with n stages of two

diodes and two capacitors, the output voltage is equal to $2n\,U_s - n(n+1)\,U_f$. The term $n(n+1)\,U_f$ represents the sum of voltage losses caused by diodes, over all capacitors on the output side (i.e. on the right side in the example – C_2 and C_4). For example if we have 2 stages like in the example, the total loss is $2+4 = 2*(2+1) = 6$ times U_f. An additional stage will increase the output voltage by twice the source voltage, minus the forward voltage drop over $2n+2$ diodes: $2U_s - (2n+2)U_f$.

Voltage doubler and tripler

A voltage doubler uses two stages to approximately double the DC voltage that would have been obtained from a single-stage rectifier. An example of a voltage doubler is found in the input stage of switch mode power supplies containing a SPDT switch to select either 120 V or 240 V supply. In the 120 V position the input is typically configured as a full-wave voltage doubler by opening one AC connection point of a bridge rectifier, and connecting the input to the junction of two series-connected filter capacitors. For 240 V operation, the switch configures the system as a

A Cockcroft-Walton voltage quadrupler circuit. It generates a DC output voltage V_o of four times the peak of the AC input voltage V_i

full-wave bridge, re-connecting the capacitor center-tap wire to the open AC terminal of a bridge rectifier system. This allows 120 or 240 V operation with the addition of a simple SPDT switch.

A voltage tripler is a three-stage voltage multiplier. A tripler is a popular type of voltage multiplier. The output voltage of a tripler is in practice below three times the peak input voltage due to their high impedance, caused in part by the fact that as each capacitor in the chain supplies power to the next, it partially discharges, losing voltage doing so.

Triplers were commonly used in color television receivers to provide the high voltage for the cathode ray tube (CRT, picture tube).

Triplers are still used in high voltage supplies such as copiers, laser printers, bug zappers and electroshock weapons.

Breakdown voltage

While the multiplier can be used to produce thousands of volts of output, the individual components do not need to be rated to withstand the entire voltage range. Each component only needs to be concerned with the relative voltage differences directly across its own terminals and of the components immediately adjacent to it.

Typically a voltage multiplier will be physically arranged like a ladder, so that the progressively increasing voltage potential is not given the opportunity to arc across to the much lower potential sections of the circuit.

Note that some safety margin is needed across the relative range of voltage differences in the multiplier, so that the ladder can survive the shorted failure of at least one diode or capacitor component. Otherwise a single-point shorting failure could successively over-voltage and destroy each next component in the multiplier, potentially destroying the entire multiplier chain.
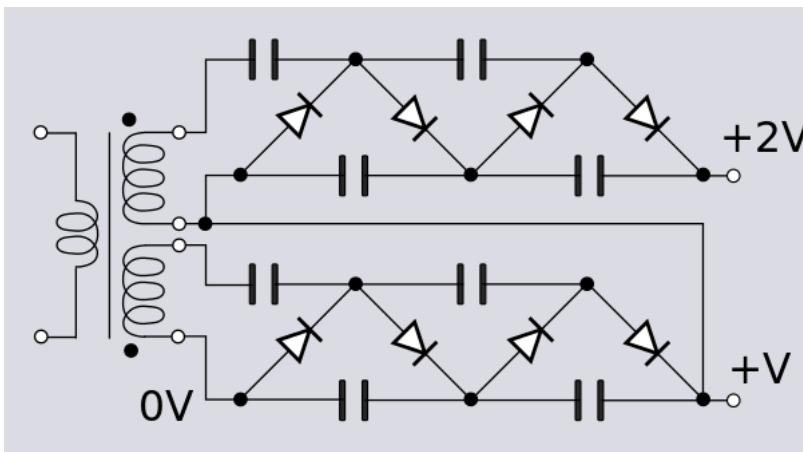
Other circuit topologies
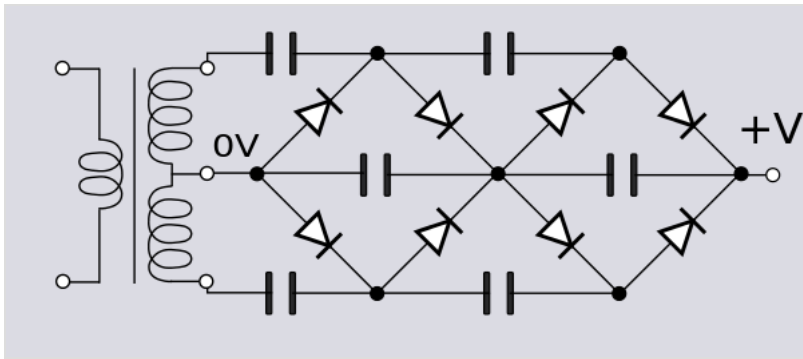
Two cascades driven by a single center-tapped transformer. This configuration provides full-wave rectification leading to less ripple and upon any collapse from arcing capacitive energy can cancel.

Stacking

A second cascade stacked onto the first one driven by a high voltage isolated second secondary winding. The second winding is connected with 180° phase shift to get full wave rectification. The two windings need to be insulated against the large voltage between them.
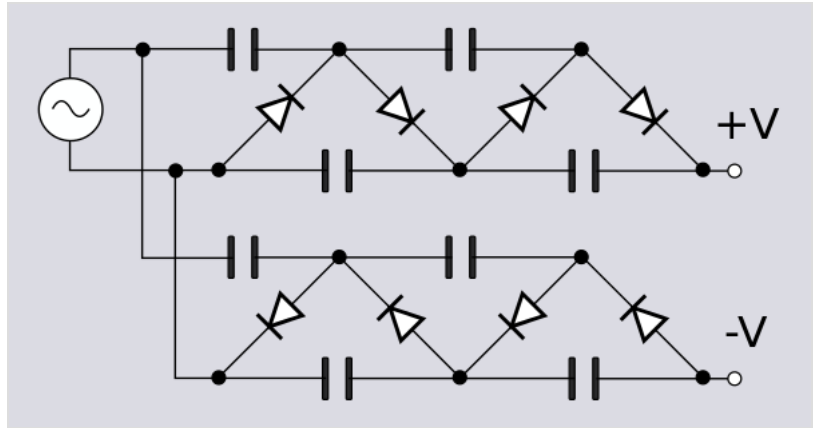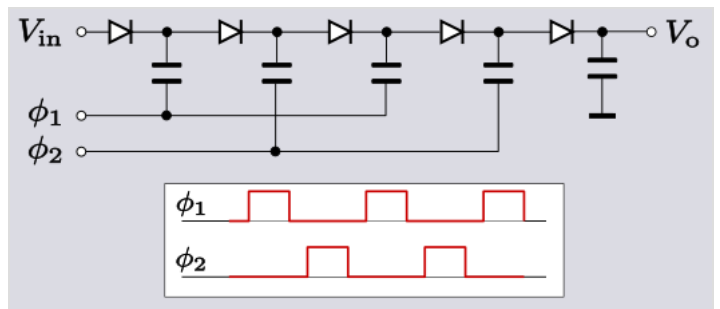
A single secondary winding of a transformer driving two cascades of opposite polarities at the same time. Stacking the two cascades provides an output of twice the voltage but with better ripple and capacitor charging characteristics than would be achieved with a single long cascade of the same voltage.

An even number of diode-capacitor cells is used in any column so that the cascade ends on a smoothing cell. If it were odd and ended on a clamping cell the ripple voltage would be very large. Larger capacitors in the connecting column also reduce ripple but at the expense of charging time and increased diode current.

Dickson charge pump

The **Dickson charge pump**, or **Dickson multiplier**, is a modification of the Greinacher/Cockcroft–Walton multiplier. There are, however, several important differences:

Standard Dickson charge pump (4 stages : 5× multiplier)

- The Dickson multiplier takes a *DC supply* as its input so is a form of DC-to-DC converter. In addition to the DC input, the circuit requires a feed of two clock pulse trains with an amplitude swinging between the DC supply rails. These pulse trains are in antiphase.[1]
- The Dickson multiplier is intended for *low-voltage applications*, unlike Greinacher/Cockcroft–Walton which is commonly used in high-voltage applications. This is because the final capacitor has to hold the entire output voltage, whereas in the Greinacher/Cockcroft–Walton multiplier, each capacitor holds at most twice the input voltage (thus easily allowing multiplication by a factor of 10 or more).
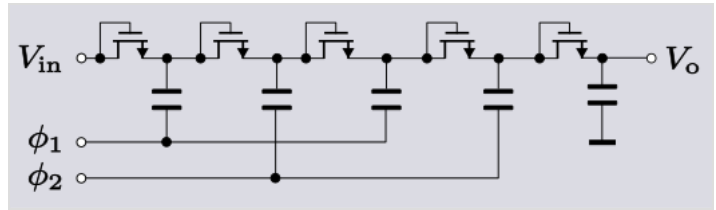
To describe the ideal operation of the circuit, number the diodes D1, D2 etc. from left to right and the capacitors C1, C2 etc. When the clock ϕ_1 is low, D1 will charge C1 to V_{in}. When ϕ_1 goes high the top plate of C1 is pushed up to $2V_{in}$. D1 is then turned off and D2 turned on and C2 begins to charge to $2V_{in}$. On the next clock cycle ϕ_1 again goes low and now ϕ_2 goes high pushing the top plate of C2 to $3V_{in}$. D2 switches off and D3 switches on, charging C3 to $3V_{in}$ and so on with charge passing up the chain, hence the name charge pump. The final diode-capacitor cell in the cascade is connected to ground rather than a clock phase and hence is not a multiplier; it is a peak detector which merely provides smoothing.[2]
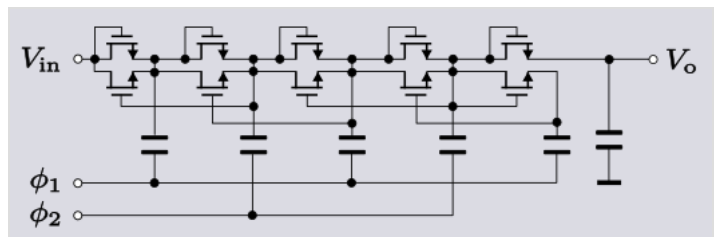
There are a number of factors which reduce the output from the ideal case of nV_{in}. One of these is the threshold voltage, V_T of the switching device, that is, the voltage required to turn it on. The output will be reduced by at least nV_T due to the volt drops across the switches. Schottky diodes are commonly used in Dickson multipliers for their low forward voltage drop, amongst other reasons. Another difficulty is that there are parasitic capacitances to ground at each node. These parasitic capacitances act as voltage dividers with the circuit's storage capacitors reducing the output voltage still further.[3] Up to a point, a higher clock frequency is beneficial: the ripple is reduced and the high frequency makes the remaining ripple easier to filter. Also the size of capacitors needed is reduced since less charge needs to be stored per cycle. However, losses through stray capacitance increase with increasing clock frequency and a practical limit is around a few hundred kilohertz.[4]

Dickson multipliers are frequently found in integrated circuits (ICs) where they are used to increase a low-voltage battery supply to the voltage needed by the IC. It is advantageous to the IC designer and manufacturer to be able to use the same technology and the same basic device throughout the IC. For this reason, in the popular CMOS technology ICs the transistor which forms the basic building

Dickson charge pump using diode-wired MOSFETs (4 stages : 5× multiplier)

block of circuits is the MOSFET. Consequently, the diodes in the Dickson multiplier are often replaced with MOSFETs wired to behave as diodes.[5]

The diode-wired MOSFET version of the Dickson multiplier does not work very well at very low voltages because of the large drain-source volt drops of the MOSFETs. Frequently, a more complex circuit is used to overcome this problem. One solution is to connect in parallel with the switching MOSFET another MOSFET biased into its linear region. This second MOSFET has a lower drain-source voltage than the switching MOSFET would have

Dickson charge pump with linear MOSFET in parallel with diode-wired MOSFET (4 stages : 5× multiplier)

on its own (because the switching MOSFET is driven hard on) and consequently the output voltage is increased. The gate of the linear biased MOSFET is connected to the output of the next stage so that it is turned off while the next stage is charging from the previous stage's capacitor. That is, the linear-biased transistor is turned off at the same time as the switching transistor.[6]
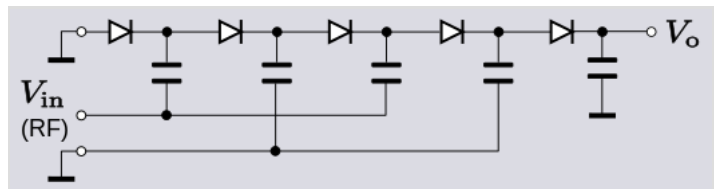
An ideal 4-stage Dickson multiplier (5× multiplier) with an input of 1.5 V would have an output of 7.5 V. However, a diode-wired MOSFET 4-stage multiplier might only have an output of 2 V. Adding parallel MOSFETs in the linear region improves this to around 4 V. More complex circuits still can achieve an output much closer to the ideal case.[7]

Many other variations and improvements to the basic Dickson circuit exist. Some attempt to reduce the switching threshold voltage such as the Mandal-Sarpeshkar multiplier[8] or the Wu multiplier.[9] Other circuits cancel out the threshold voltage: the Umeda multiplier does it with an externally provided voltage[10] and the Nakamoto multiplier does it with internally generated voltage.[11] The Bergeret multiplier concentrates on maximising power efficiency.[12]
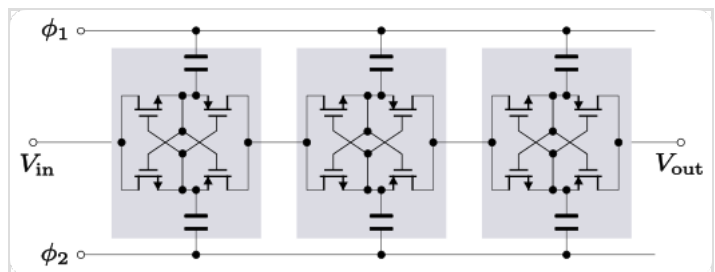
Modification for RF power

In CMOS integrated circuits clock signals are readily available, or else easily generated. This is not always the case in RF integrated circuits, but often a source of RF power will be available. The standard Dickson multiplier circuit can be modified to meet this requirement by simply grounding the normal input and

Modified Dickson charge pump (2 stages : 3× multiplier)

one of the clock inputs. RF power is injected into the other clock input, which then becomes the circuit input. The RF signal is effectively the clock as well as the source of power. However, since the clock is injected only into every other node the circuit only achieves a stage of multiplication for every second diode-capacitor cell. The other diode-capacitor cells are merely acting as peak detectors and smoothing the ripple without increasing the multiplication.[13]

Cross-coupled switched capacitor

A voltage multiplier may be formed of a cascade of voltage doublers of the cross-coupled switched capacitor type. This type of circuit is typically used instead of a Dickson multiplier when the source voltage is 1.2 V or less. Dickson multipliers have increasingly poor power conversion efficiency as the input voltage drops because the voltage drop across the diode-wired transistors becomes much more significant compared to the output

Cascade of cross-coupled MOSFET voltage doublers (3 stages : 4× multiplier)

voltage. Since the transistors in the cross-coupled circuit are not diode-wired the volt-drop problem is not so serious.[14]

The circuit works by alternately switching the output of each stage between a voltage doubler driven by ϕ_1 and one driven by ϕ_2. This behaviour leads to another advantage over the Dickson multiplier: reduced ripple voltage at double the frequency. The increase in ripple frequency is advantageous because it is easier to remove by filtering. Each stage (in an ideal circuit) raises the output voltage by the peak clock voltage. Assuming that this is the same level as the DC input voltage then an n stage multiplier will (ideally) output nV_{in}. The chief cause of losses in the cross-coupled circuit is parasitic capacitance rather than switching threshold voltage. The losses occur because some of the energy has to go into charging up the parasitic capacitances on each cycle.[15]

Applications

The high-voltage supplies for cathode-ray tubes (CRTs) in TVs often use voltage multipliers with the final-stage smoothing capacitor formed by the interior and exterior aquadag coatings on the CRT itself. CRTs were formerly a common component in television sets. Voltage multipliers can still be found in modern TVs, photocopiers, and bug zappers.[16]

High voltage multipliers are used in spray painting equipment, most commonly found in automotive manufacturing facilities. A voltage multiplier with an output of about 100kV is used in the nozzle of the paint sprayer to electrically charge the atomized paint particles which then

get attracted to the oppositely charged metal surfaces to be painted. This helps reduce the volume of paint used and helps in spreading an even coat of paint.

A common type of voltage multiplier used in high-energy physics is the Cockcroft–Walton generator (which was designed by John Douglas Cockcroft and Ernest Thomas Sinton Walton for a particle accelerator for use in research that won them the Nobel Prize in Physics in 1951).
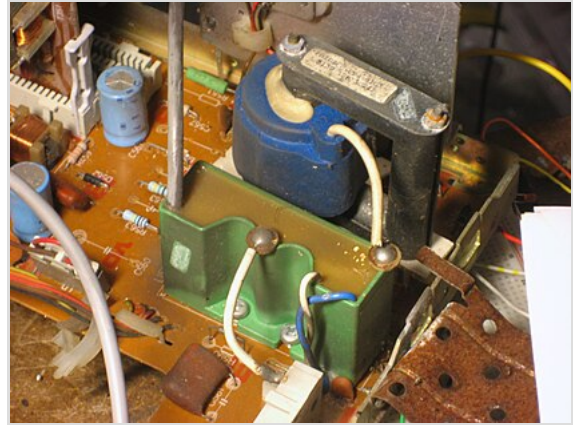
TV cascade (green) and flyback transformer (blue).

See also

- Marx generator (a device that uses spark gaps instead of diodes as the switching elements and can deliver higher peak currents than diodes can).
- Boost converter (a DC-to-DC power converter that steps up voltage, frequently using an inductor)

Notes

1. Liu, p. 226
   Yuan, p. 14
2. Liu, pp. 226–227
3. Yuan, pp. 13–14
   Liul2006, pp. 227–228
4. Peluso *et al.*, p. 35
   Zumbahlen, p. 741
5. Liu, pp. 226–228
   Yuan, p. 14
6. Liu, pp. 228–230
   Yuan, pp. 14–16
7. Yuan, pp. 14–16
8. Yuan, pp. 17–18
9. Liu, pp. 230–232
10. Yuan, pp. 18–20
11. Yuan, pp. 19–20
12. Yuan, pp. 20–21
13. Liu, pp. 228–230
    Yuan, pp. 14–15
14. Campardo *et al.*, pp. 377–379
    Liu, pp. 232–235
    Lin, p. 81
15. Campardo *et al.*, p. 379
    Liu, p. 234
16. McGowan, p. 87

Bibliography

- Campardo, Giovanni; Micheloni, Rino; Novosel, David *VLSI-design of Non-volatile Memories*, Springer, 2005 ISBN 3-540-20198-X.
- Lin, Yu-Shiang *Low Power Circuits for Miniature Sensor Systems*, Publisher ProQuest, 2008 ISBN 0-549-98672-3.
- Liu, Mingliang *Demystifying Switched Capacitor Circuits*, Newnes, 2006 ISBN 0-7506-7907-7.
- McGowan, Kevin, *Semiconductors: From Book to Breadboard*, Cengage Learning, 2012 ISBN 1133708382.
- Peluso, Vincenzo; Steyaert, Michiel; Sansen, Willy M. C. *Design of Low-voltage Low-power CMOS Delta-Sigma A/D Converters*, Springer, 1999 ISBN 0-7923-8417-2.
- Yuan, Fei *CMOS Circuits for Passive Wireless Microsystems*, Springer, 2010 ISBN 1-4419-7679-5.
- Zumbahlen, Hank *Linear Circuit Design Handbook*, Newnes, 2008 ISBN 0-7506-8703-7.

External links

- Basic multiplier circuits (http://www.kronjaeger.com/hv/hv/src/mul/)
- Cockcroft Walton multipliers (http://blazelabs.com/e-exp15.asp)
- Schematic of Kadette brand (International Radio Corp.) model 1019 (http://www.nostalgiaair.org/PagesByModel/503/M0009503.pdf). A 1937 radio with a vacuum tube (25Z5) voltage multiplier rectifier.

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